ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	METHODS AND APPARATUS FOR DEFECT ISOLATION

Application Number :

Confirmation Number:

First Named Applicant: Leendert Huisman

Attorney Docket Number: BUR920030066US1

Art Unit:

Examiner:

Search string: (3761695 or 6308290 or 6490702 or 6516432).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
SA	1	3761695	1973-09-25	Eichelberger			
SA	2	6308290	2001-10-23	Forlenza et al.			
SA	3	6490702	2002-12-03	Song et al.			
SA	4	6516432	2003-02-04	Motika et al.			

Signature

Examiner Name	Date
Shawn Ae	11/08/06

Sheet 1 of 1 sheet

U.S. Department of Commerce, Patent and Trademark Office	Docket No.: BUR920030066US1	Serial No.: 10/708,380
LIST OF RELEVANT ART CITED BY APPLICANT (Use several sheets if necessary)	Applicant(s): Leendert M. Huisman et al.	
	Filing Date: February 27, 2004	Group: unknown

U.S. Patent Documents

*Examiner Initial		Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						

Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AG							
	AH							
	AI							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EA	AJ	E.B. Eichelberger, et al, "A Logic Design Structure for LSI Testability", Proceedings of the Fourteenth Design Automation Conference, New Orleans, 1977, pps. 462-468.
EA	AK	David P. Vallett, "IC Failue Analysis: The Importance of Test and Diagnostics", IEEE Design & Test of Computers, July-September 1997, pps. 76-82.
EA	AL	James L. Schafer et al. "Partner SRLS for Improved Shift Register Diagnostics", IEEE VLSI Test Symposium, June 1992, pps. 198-200.
EA	AM	Sandip Jundu, "Diagnosing Scan Chain Faults", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 2, No. 4, December 1994, pps. 512-517.
EA	AN	Samantha Edirisooriya et al., "Diagnosis of Scan Path Failures", Proceedings of IEEE VLSI Test Symposium April 1995, pps. 250-255.
EA	AO	Sridhar Narayanan et al., "An Efficient Scheme to Diagnose Scan Chains", International Test Conference, July 1997, pps. 704-713.

Examiner Essaw Abebe Date Considered 11/08/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

C:\WP51\FORMS\1449.PTO 1/94

Express Mail Label No.: